# POSSIBILITY OF SILICON MONOLITHIC MILLIMETERWAVE INTEGRATED CIRCUITS

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## ABSTRACT

Previous work on high resistivity silicon suggests that microstrip line dielectric losses cease to be significant above 30 GHz. Silicon-Germanium Heterojunction Bipolar Transistors now provide a well behaved three-terminal device capable of operating at microwave frequencies. The tradeoffs available to operate this device at millimeterwave frequencies are discussed, making the fabrication of Silicon Monolithic Millimeterwave Integrated Circuits a genuine possibility.

## INTRODUCTION

The choice of GaAs for Monolithic Microwave Integrated Circuits has been dictated by its properties: semi-insulating substrates are readily available, three terminal amplifying and oscillating devices are currently available to over 100 GHz. But problems in manufacture remain: the quality of the material is variable, the yields are not as high as may be expected, and the circuits are expensive. Silicon as a microwave substrate material is lossy, but it has been shown that for frequencies above 30 GHz, the "dielectric" loss due to the low resistivity (2,000 to 10,000 ohm-cm) ceases to be a problem[1]. However, apart from Schottky-barrier and p-n junction diodes, the Impatt diodes appeared to be the only active amplifying device available in this material. While Impatt diodes currently provide the best solid state high power sources at the present time, they are exceedingly difficult to match in the monolithic circuit context. Thus, there is considerable reluctance to use these devices in Integrated Circuits. The advent of the Silicon-Germanium Heterojunction Bipolar Transistor (Si-Ge HBT) provides a three-terminal device which is well behaved and capable of working at millimeterwave frequencies. We provide an analysis to show that, indeed, these devices may be the choice for Silicon-based Millimeterwave Integrated Circuits. In the following section, the performance of these Si-Ge HBTs are analyzed, and we show that $f_{max}$ in the region of 100 GHz may be feasible with these devices. Thus, millimeterwave ICs in Silicon are a possible alternative to GaAs and InP based circuits. The advantages of Silicon in device and circuit processing are obvious and will not be documented here.

## PERFORMANCE OF THE GE-Si HBT

It has been demonstrated that molecular beam epitaxy may be used to fabricate heterojunctions of $Ge_xSi_{1-x}$ on Si. While not lattice matched, the Ge-Si layer will grow pseudomorphically up to a critical layer thickness at which gross stress relief will occur via the formation of dislocations[2]. This technique with thin dislocation free layers has been used to fabricate HBTs with modest success[3]. More recently, a vapor phase approach to the fabrication has produced devices with exceptional results: current gains of 400 have been obtained and ideal Gummel plots remain down to a picoampere of base current[4]. It is of interest then, to predict the microwave performance of the devices that may be fabricated from such layers. It is important to emphasize that these are first order estimates of transistor performance. All the material properties of the Ge-Si layer except the band gap will be assumed to be those of silicon.

Figure 1 shows a super self-aligned transistor (SST), a device structure that has been developed for digital applications, but can also be used to fabricate microwave Ge-Si HBT's. A 2000Å moderately doped (1E+17 $cm^{-3}$) collector is first grown on a heavily doped substrate or buried layer. A thick field oxide is then grown in a local oxidation process and a 1000Å sub poly oxide is grown. Next 2500Å of $p^{++}$ polysilicon is deposited and oxidized to 1000Å. The oxide/poly sandwich is anistropically patterned. The base contacts are formed through an oxide undercut followed by an undoped poly CVD plug fill and poly oxidation to form the sidewall oxide spacers. Using the vapor phase chemistry and the lower growth nucleation rate on the oxide, selective growth is now performed to form the base and emitter regions. Finally, a thicker $N^{++}$ polysilicon is deposited and patterned to contact the emitter. The base doping is set at 5E+18 $cm^{-3}$, this represents a realistic estimate of the maximum boron doping achievable at the Ge-Si growth temperature. The emitter doping concentration is also set to 5E+18 $cm^{-3}$; this represents a trade off between DC current gain and EB capacitance. Due to the heterojunction such a device should still have $\beta$ greater than 100. We shall assume that the transistor has an interdigitated structure with 20 fingers of 50 $\mu$m length.

The critical layer thickness as a function of the Ge mole fraction has been determined by People[5] among others. For the purpose of this calculation we shall select a base width of 500Å and an alloy



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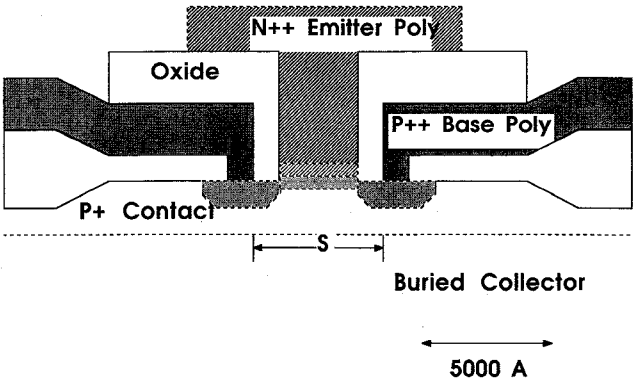


Figure 1. Super Self Aligned HBT Structure shown with a 0.5 μm emitter cut (0.3 μm emitter).

concentration of $Ge_{.25}Si_{.75}$, although this choice is somewhat arbitrary. The band offset of the heterointerface is a critical function of the strain in the pseudomorphic layer. The presence of a thin silicon cladding layer has been demonstrated to shift[5] the offset fom -0.02 eV to +0.15 eV. In any case, the majority of the bandgap discontinuity appears in the valence band. Since we cannot predict with any accuracy the offset, we shall model this by putting all of the discontinuity (150 eV) at the valence band edge. The effect of this offset is to increase the device current gain by providing an effective barrier for hole injection into the emitter, while minimizing any effects due to hot electron injection into the base.

Assuming $\alpha \simeq 1$, we can now calculate $f_{max}$, the frequency at which the unilateral gain becomes unity from:

$$f_{max} = (16\pi^2 r_B C_C (t_{EC} + r_E C_C))^{-1/2}$$

where $r_B$ is the base resistance, $r_E$ is the emitter resistance, and $C_C$ is the collector capacitance. $t_{EC}$, the device transit time, can be found from

$$t_{EC} = t_E + t_B + t_C + t'_C.$$

where $t_B$ is the emitter-base depletion layer charging time, $t_B$ is the base charging time, $t_C$ is the transit time the base-collector depletion layer, and $t_C$ is the RC delay of the collector. For a heavily doped buried collector $t'_C$ is negligible. $t_C$ can be approximated by dividing the depletion layer thickness by twice the saturation velocity. The base charging time is given by

$$t_B = W^2/\eta D_e \quad ,$$

where W is the pinched base width and $D_e$ is the diffusivity of the minority carrier electrons in the base. Assuming the values for Silicon concentration dependent diffusivity and taking $\eta = 2$ for a uniform base concentration, $t_B$ is typically less than .01 psec. The emitter base depletion layer charging time is given by

$$t_E = r_E(C_E + C_C + C_{par}),$$

where $r_E$ is the small signal emitter resistance, $C_E$ is the emitter base capacitance, $C_C$ is the base collector capacitance, and $C_{par}$ is the total parasitic capacitance.

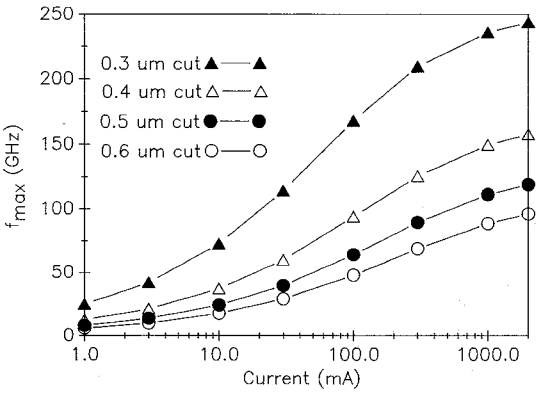


Figure 2. Calculated $f_{max}$ as a function of the DC collector current with emitter stripe cut width as a parameter.

Figure 2 shows a plot of the calculated $f_{max}$ versus emitter current for the proposed super self-aligned device with several drawn strip widths. Initially, the performance improves sharply with increasing current due to the reduced emitter charging time. At higher currents the curve saturates due to the effects of the $r_E * C_C$ terms in the denominator. If we reduce the drawn stripe width and hold the sidewall oxide constant at 0.1 mm per side, a substantial improvement results with the highest predicted $f_{max}$ values well over 100 GHz. Due to base push out however, these predicted maximum values are somewhat optimistic. We can estimate the onset of the Kirk effect using

$$I_K = q N_C v_s A_E$$

where $N_C$ is the collector doping density, $v_s$ is the saturation velocity, and $A_E$ is the emitter area. We then predict more realistic maxima are 60 GHz at 210 mA for the 0.6 um drawn stripe, 70 GHz at 160 mA for the 0.5 um drawn stripe, 95 GHz at 105 mA for the 0.4 um drawn stripe, and 135 GHz at 50 mA for the 0.3 um drawn stripe. It should be emphasized that this high performance results primarily from the fine lithography and advanced device structure assumed. In a recent paper where 1.0 um lithography and a less aggressive structure are assumed, the predicted values for $f_{max}$ are about 35 GHz[6]. If we assume their device parameters our model agrees within approximately 10%.

## CONCLUSIONS

The above calculations suggest the Silicon-Germanium HBTs are possible candidates as three terminal devices at millimeterwave frequencies. Devices built on high resistivity silicon will then allow the fabrication of Monolithic Integrated Circuits in Silicon at frequencies above well 30 GHz.

REFERENCES

(1) A. Rosen, M. Caulton, P. Tabile, A. M. Gombar, W. M. Janton, C. P. Wu, J. F. Corby, C. W. Magee, RCA Review, 42, 633 (1981)

(2) J. C. Beam, L. C. Feldman, A. T. Fiory, S. Nakahara, and I. K. Robinson, J. Vac. Sci. Technol. A2, 436 (1984)

(3) S. S. Iyer, G. L. Patton, S. S. Delage, S. Tiwari, and J. M. C. Stork, Proc. of the 1987 IEDM, Washington, DC (1987)

(4) C. A. King, J. L. Hoyt, C. M. Gronet, J. F. Gibbons, M. P. Scott, S. J. Rosner, G. Reid, S. Laderman, K. Nauka, and T. I. Kamins, Proc of the 1988 DRC/MRC, VB-7 (1988)

(5) R. People and J. C. Bean, Appl. Phys. Lett. 48, 538 (1986)

(6) T. Wok and H. Morkoc, IEEE Trans. Elec. Dev. 10, 33 (1989)